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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,371	07/02/2003	Jan Paul Anthonie Van der Wagt	INPH1-P065	3713
7590 05/12/2004			EXAMINER	
Fernandez & Associates, LLP			TON, MY TRANG	
PO Box D			ART UNIT	
Menlo Park, CA 94026-6402			PAPER NUMBER	
			2816	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/612,371

**Applicant(s)**VAN DER WAGT, JAN PAUL  
ANTHONIE**Examiner**

My-Trang N. Ton

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16, 22-36 and 39-45 is/are rejected.
- 7) ☒ Claim(s) 17-21, 37 and 38 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 05/07/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Drawings***

Figures 2 and 3A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

Claim 43 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form.

### ***Claim Rejections - 35 USC § 112***

Claims 14-16 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "the step of preconditioning" in line 1. There is insufficient antecedent basis for this limitation in the claim.

In claim 15, the limitation "the step of preconditioning the signal comprises the step of preconditioning the signal input to the differential pair module" is redundant recited with claim 14.

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Claim 16 recites the limitation "the stage driving" in line 2. There is insufficient antecedent basis for this limitation in the claim.

In claim 36, it is unclear which element is referred as "a keep alive transistor". In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings. Moreover, "a keep alive transistor" and "a bleed resistor" are left dangling.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-5, 8-13, 22-30, 32-33, 36, 39-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Schuler et al (U.S Patent No. 6,246,269).

Schuler et al disclose in Fig. 2 a programmable damping for write circuits including:

establishing a cascode transistor module (Q9, Q10) for receiving a substantially differential current signal from a differential pair module (Q1-Q4) and transmitting the substantially differential current signal into a pair of external load (R3A, R4A, R3B, R4B) impedances as a first output waveform (connected to node N1) and a second output wave form (connected to node N2); and

engineering the resistive loads (R5, R6) seen by the output nodes (connected to N1, N2) of the differential pair module (Q1-Q4), based on one or more criteria thereby

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engineering the symmetry between the rising and the falling edge for each of the first output waveform and the second output waveform as recited in claim 1.

The cascode transistor module (Q9, Q10) comprises bipolar transistors as recited in claim 2.

The differential pair module (Q1, Q3) comprises bipolar transistors as recited in claim 4.

The output nodes of the differential pair module (Q1-Q4) comprise the collector nodes of the bipolar transistors (Q4, Q2) and the input nodes (Vy, Vr) of the differential pair module (Q1-Q4) comprise the base nodes of the bipolar transistors (Q4, Q2) as recited in claim 5.

The step of engineering the resistive loads (R5, R6) comprises the step of inserting a first resistive module (R5, R6) between the cascode transistor module (Q9, Q10) and the differential pair module (Q1-Q4) as recited in claim 8.

The first resistive module comprises a first resistor (R5) and a second resistor (R6) in a parallel configuration as recited in claim 9.

The first (R5) and the second resistor (R6) have substantially identical characteristics as recited in claim 10.

The step of engineering the resistive loads comprises the step of selecting a cascode bias voltage (bias voltage connected to V3, Vcc, S3) for the cascode transistor module (Q9, Q10) as recited in claim 11.

The method recited in claims 12-13, 22-23 are inherently seen in Fig. 2 of Schuler et al.

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Claim 24 is similarly rejected as claim 1:

a cascode transistor module (Q9, Q10) for receiving a substantially differential current signal from a differential pair module (Q1-Q4) and transmitting the substantially differential current signal into a pair of external load (R3A, R4A, R3B, R4B) impedances as a first output waveform (connected to N1) and a second output waveform (connected to N2) wherein the cascode transistor module comprises:

a resistive load (R5, R6) at the input nodes of the cascode transistor module; and

a cascode bias voltage node (connected to V3, VCC, S3) for applying a cascode bias voltage wherein the symmetry between the rising edge and the falling edge for each of the first output waveform (connected to N1) and the second output waveform (connected to N2) may be altered by careful selection of one or more elements selected from the list of:

the resistive load (R5, R6) and

the cascode bias voltage (connected to V3, Vcc, S3).

The resistive load (R5, R6) at the input nodes of the cascode transistor module are due to the intrinsic properties of the transistor elements (Q9, Q10) as recited in claim 25.

Elements R5 and R6 read on a first resistive module as recited in claim 26.

The first resistive module comprises a first resistor (R5) and a second resistor (R6) in a parallel configuration as recited in claim 27.

The first resistor (R5) and the second resistor (R6) have substantially identical characteristics as recited in claim 28.

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The limitation recited in claim 29 is seen to read directly in Fig. 2.

The cascode transistor module (Q9, Q10) comprises bipolar transistors as recited in claim 30.

The differential pair module (Q1-Q4) comprises bipolar transistors as recited in claim 32.

The output nodes of the differential pair module (Q1-Q4) comprise the collector nodes of the bipolar transistors (Q4, Q2) and the input nodes (Vy, Vr) of the differential pair comprise the base nodes of the bipolar transistors (Q4, Q2) as recited in claim 33.

Insofar as understood, element Q7A reads on a keep alive transistor as recited in claim 36.

Element LH reads on one inductive modules coupled to the outputs (connected to node N1, N2) of the cascode transistor module (Q9, Q10) as recited in claim 39.

Element R1 reads on a second resistive module and element R2 reads on a third resistive module as recited in claim 40.

The second resistive module (R1) and the third resistive (R2) are substantially identical as recited in claim 41.

The second resistive module (R1) and the third resistive (R2) comprise one or more resistors as recited in claim 42.

Under broader reasonable interpretation, elements S1, S2, Q7A, Q8A, Q7B, Q8B are seen as one or more devices as recited in claim 43.

***Claim Rejections - 35 USC § 103***

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 6-7, 31, 34-35, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuler et al as applied to claims 1 and 24 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Schuler. However, this reference does not show the “cascode transistor module comprises field effect transistors” (claims 3, 31), “differential pair module comprises field effect transistors” (claims 6, 34); “output nodes of the differential pair ... of said field effect transistors” (claims 7, 35); “devices comprises one or more selected from the list of: broad-band amplifiers ... oscillators” (claim 44) or “the list of “wireless local area networks ... high-speed communication systems” (claim 45).

Regarding the “field effect transistors” limitation, field effect transistors are well-known switching devices and patentable equivalent to bipolar transistors since no unobvious results are seen produce from there use. Therefore, it would have been obvious at the time of the invention was made for one skilled in the art to utilize these particular types of transistors because of this well-known advantages in performance and integration.

Regarding the selected list recited in claims 44-45, this specific limitation drawn to the choice of devices is seen as design expedients dependent upon the desired results. With the advance of today’s technology, it would have been obvious at the time

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of the invention was made for one skilled in the art to realize the circuit of Schuler circuit can be implemented through the particular type of devices for the purpose producing correspondingly different output values.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



MY-TRANG NUTON  
PRIMARY EXAMINER

May 7, 2004